

Notes on the Measured S-parameters for the F1241 Dual Intermediate Frequency Digital Variable Gain Amplifier

Introduction

The F1241 Dual Intermediate Frequency Digital Variable Gain Amplifier consists of two separate channels. Each channel has a differential digital step attenuator (DSA) and an differential amplifier. The DSA is a 6-bit device with a 1.0 dB step for a 31.0 dB attenuation range. The amplifier has a maximum differential gain of approximately 20 dB. When discussing the F1241 we talk about the gain state which will vary from 20 to -11.0 dB. The frequency range 10 to 500 MHz.

We have designed our evaluation board for single ended operation for ease of testing. This means we use a 4:1 transformer to transmit a signal into and out of the DVGA. Customers are requesting S-parameters to the individual ports on the package so that simulations can be done at the system level. This note is to explaining the calibration and testing methodology that has been performed to obtain the data.

Evaluation Board

In order to accomplish this, a new evaluation board was designed. Figure 1 shows the original evaluation board, while Figure 2 shows the special evaluation board.

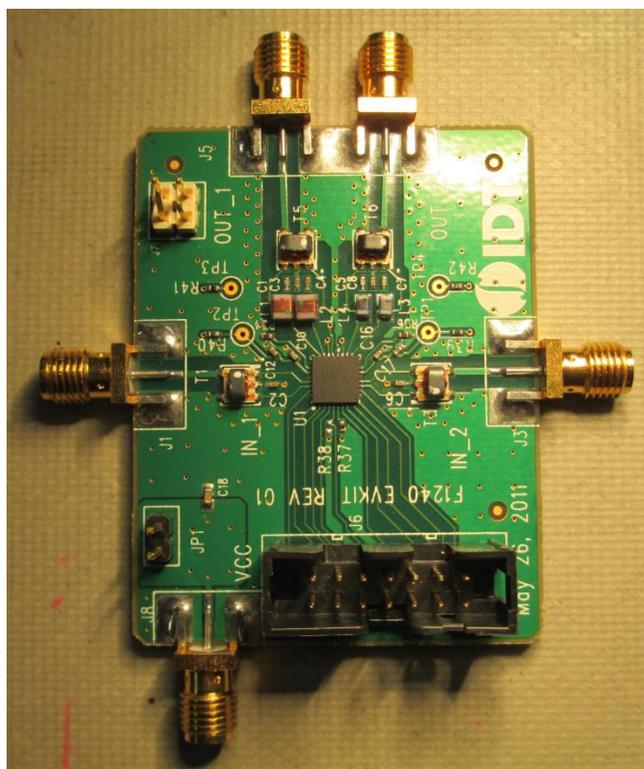


Figure 1 - Standard F1241 Evaluation Board

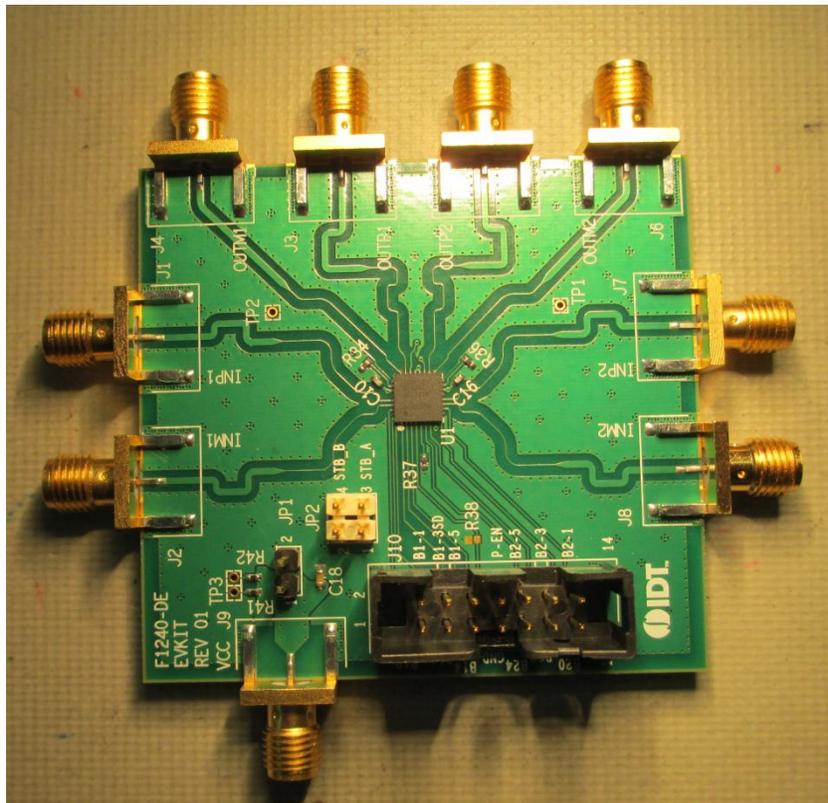


Figure 2 - Modified F1241 Evaluation Board for Individual Port Access

The new evaluation board has equal length lines. The miter bends were needed to create the proper length. The overall lengths were matched to within 10 mils or 1.3 degrees at 1.0 GHz. This error is attributed to not properly accounting for the miter bend effective length. But does not affect the overall calibration. We only need one board to make a complete measurement. This evaluation board was mislabeled for the port names. “P” and “N” should be reversed. This has no effect on the measurements.

Calibration

The above board was designed so that a port reference calibration can be preformed. Details of this technique can be found at Keysight Technologies (formerly Agilent Technologies) website in their application notes and forums. A simplified description is the network analyzer is first calibrated to the connectors using standard calibration (mechanical or electronic) techniques. Then the evaluation board is connected to network analyzer with no device installed. This yields a “device” which the connector transmission line and an open circuit. By using the port reference and taking into account phase, loss and mismatch the calibration is modified to move the reference plane from the end of the cable to the open circuit. This technique is best suited for frequency below 1 GHz.

Since the amplifier is a differential amplifier there are four ports that need be measured, so a four port calibration was performed from 0.005 to 1.000 GHz. The input power was set for -10 dBm to assure that the small signal operation of the amplifier was being used.

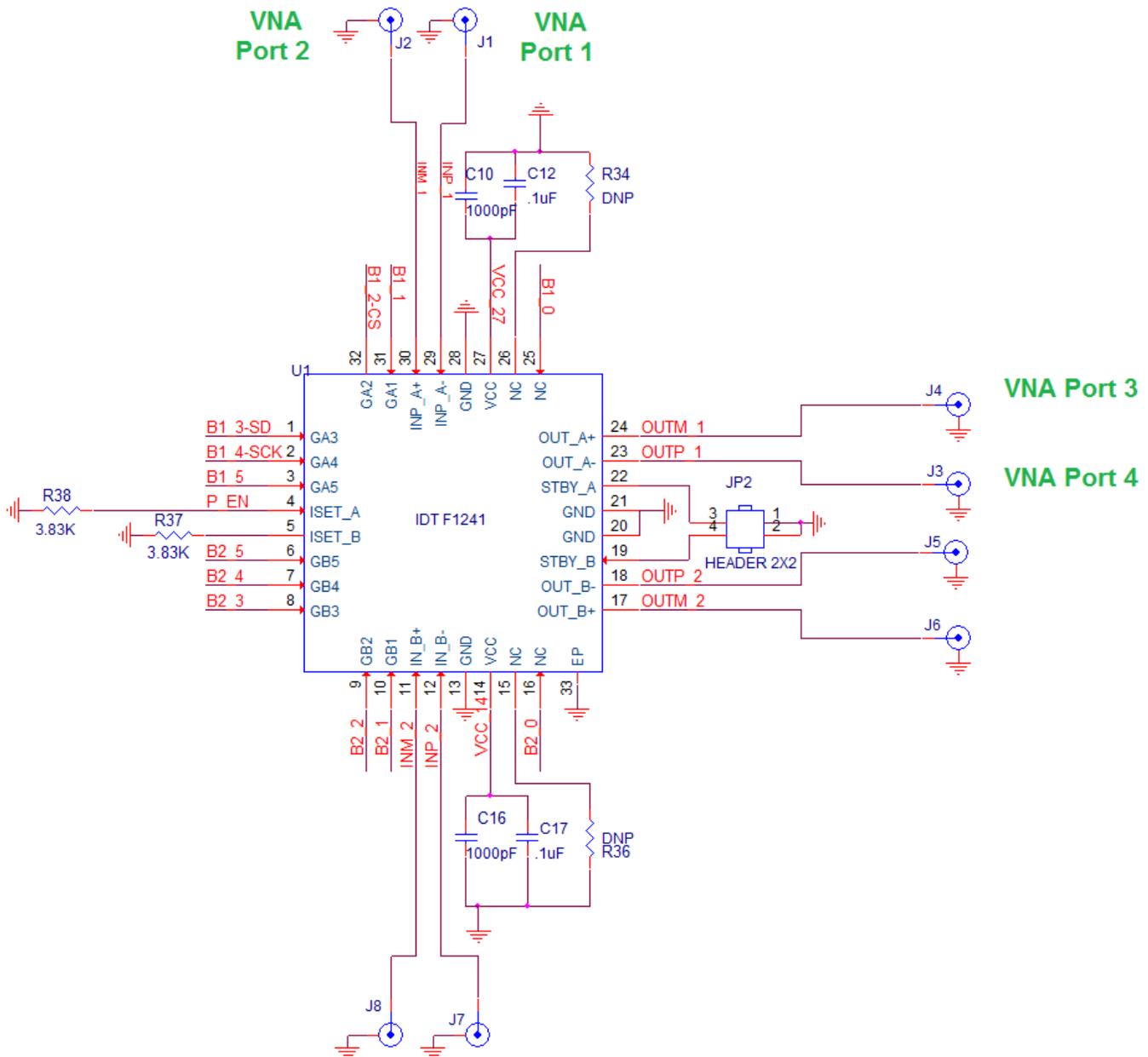


Figure 3 - Network Analyzer Port Connection and S-Parameter

Data Collection

All gain states of the F1241 were measured. Only Channel 1 (or “A”) was measured. Figure 3 shows how the network analyzer was connected to the product. The port designations also represent the ports within the S-parameter files. The states were changed by using the Parallel Interface. The parallel bits used are shown in Table.

The S-parameter data is single ended data and reference to 50 ohms. To evaluate differential or common mode gain, impedances, and other parameters the S-parameter files may be used in a linear simulator that will apply the correct signals to both ports 1 and 2 and ports 3 and 4.

Table 1 - F1241 States, Filenames, and Control Word

State	Gain State	File Name	D4	D3	D2	D1	D0
0	20.0	F1241_p20p0dB_SE.S4P	0	0	0	0	0
1	19.0	F1241_p19p0dB_SE.S4P	0	0	0	0	1
2	18.0	F1241_p18p0dB_SE.S4P	0	0	0	1	0
3	17.0	F1241_p17p0dB_SE.S4P	0	0	0	1	1
4	16.0	F1241_p16p0dB_SE.S4P	0	0	1	0	0
5	15.0	F1241_p15p0dB_SE.S4P	0	0	1	0	1
6	14.0	F1241_p14p0dB_SE.S4P	0	0	1	1	0
7	13.0	F1241_p13p0dB_SE.S4P	0	0	1	1	1
8	12.0	F1241_p12p0dB_SE.S4P	0	1	0	0	0
9	11.0	F1241_p11p0dB_SE.S4P	0	1	0	0	1
10	10.0	F1241_p10p0dB_SE.S4P	0	1	0	1	0
11	9.0	F1241_p09p0dB_SE.S4P	0	1	0	1	1
12	8.0	F1241_p08p0dB_SE.S4P	0	1	1	0	0
13	7.0	F1241_p07p0dB_SE.S4P	0	1	1	0	1
14	6.0	F1241_p06p0dB_SE.S4P	0	1	1	1	0
15	5.0	F1241_p05p0dB_SE.S4P	0	1	1	1	1

State	Gain State	File Name	D4	D3	D2	D1	D0
16	4.0	F1241_p04p0dB_SE.S4P	1	0	0	0	0
17	3.0	F1241_p03p0dB_SE.S4P	1	0	0	0	1
18	2.0	F1241_p02p0dB_SE.S4P	1	0	0	1	0
19	1.0	F1241_p01p0dB_SE.S4P	1	0	0	1	1
20	0.0	F1241_p00p0dB_SE.S4P	1	0	1	0	0
21	-1.0	F1241_m01p0dB_SE.S4P	1	0	1	0	1
22	-2.0	F1241_m02p0dB_SE.S4P	1	0	1	1	0
23	-3.0	F1241_m03p0dB_SE.S4P	1	0	1	1	1
24	-4.0	F1241_m04p0dB_SE.S4P	1	1	0	0	0
25	-5.0	F1241_m05p0dB_SE.S4P	1	1	0	0	1
26	-6.0	F1241_m06p0dB_SE.S4P	1	1	0	1	0
27	-7.0	F1241_m07p0dB_SE.S4P	1	1	0	1	1
28	-8.0	F1241_m08p0dB_SE.S4P	1	1	1	0	0
29	-9.0	F1241_m09p0dB_SE.S4P	1	1	1	0	1
30	-10.0	F1241_m10p0dB_SE.S4P	1	1	1	1	0
31	-11.0	F1241_m11p0dB_SE.S4P	1	1	1	1	1